Amendments to the Specification:

Please amend the specification as follows:

Insert before the first line, the following sentence:

This application is a continuation application of co-pending application Serial Number 09/708,339, filed on November 8, 2000, which is a continuation of prior application Serial Number 09/087,017, filed on May 29, 1998, now U.S. Patent No. 6,167,245, which are each hereby incorporated by reference in its entirety.

On Page 22, in the second paragraph:

FIG. 14 is a block diagram of an alternative embodiment 1400 for achieving dual band operation for VCO 612. A second switch (SW) 1410 is used to select either a first VCO (VCO1) 612A or a second VCO (VCO2) 612B. A first external inductor (L_{RF1}) 1416 may be selected so that the VCO1 612A has an RF output (RF1) ~~1416~~ 1412 centered in a first desired frequency band. Similarly, a second external inductor (L_{RF2}) 1418 may be selected so that the VCO2 612B has an RF output (RF2) 1414 centered in a second desired frequency band. The selected frequency is connected through switch 1410 to provide the desired output frequency (f_{OUT}) 102. Power to the non-used VCO 612A or 612B may be shut down, for example by starving the circuit of current from a current generator. This multiple VCO arrangement according to the present invention eliminates potential sources of phase noise by moving the switch (SW) 1410 outside of the LC tank. This approach may also be used to implement any desired number of frequency bands by adding additional VCOs, inductors, and switches (or multiplexers).

On Pages 26-27, in the paragraph beginning at the bottom of Page 26:

As depicted in FIG. 5, the discrete control block 502 provides the digital control word (B_C) 404 as an output. The discrete control block 502 may perform any desired procedure to determine how to adjust the digital control word (B_C) 404 to coarsely tune the output frequency. Potential procedures include non-linear control algorithms and linear control algorithms. For example, a non-linear control algorithm could be implemented in which a simple "too fast" or "too slow" frequency comparison determination is made between the divided output frequency

(f_{OUT}/N) ~~216~~ 218 and the divided reference frequency (f_{REF}/R) ~~218~~ 216, and the digital control block 502 may use a successive approximation algorithm to coarsely tune the output frequency (f_{OUT}) 102. Alternatively, a linear control algorithm could be implemented in which a quantitative frequency comparison determination is made about the approximate size of the frequency error between the divided output frequency (f_{OUT}/N) ~~216~~ 218 and the divided reference frequency (f_{REF}/R) ~~218~~ 216, and the control block 812 may change the digital control word (B_C) 404 by an appropriate amount to compensate for the size of the frequency error. It is noted that the procedure used may depend upon numerous variables including the particular application involved and the level of coarse tuning desired.

On Page 29, in the first full paragraph:

In TABLE 2 below, an example procedure for control block 812 is described in more detail for controlling the digital control word (B_C) 404. This procedure correlates to the capacitor weighting scheme set forth in TABLE 1 in which the number of capacitor/switch circuits was selected to be eleven. The number of bits in the digital control word (B_C) 404 has also been chosen to be eleven. It is noted that the procedure implemented will depend upon design considerations and that any desired procedure may be implemented. Like TABLE 1, TABLE 2 below was contemplated for a dual band cellular phone application as depicted and described with respect to FIGS. 6A and 6B above. As discussed above, capacitors are added by changing their respective control bit to a "1" ~~and a dropped~~ and are dropped by changing their respective control to a "0". (If PMOS transistor switch circuits were utilized instead of NMOS transistor switch circuits, these control bits would of course change accordingly so that a "0" would add in the capacitor and a "1" would drop the capacitor.)

On Page 32, in the first full paragraph;

For each frequency comparison, if the level is high (logic level "1"), the comparison signal 811 to control block 812 that the divided output frequency (f_{OUT}/N) ~~216~~ 218 is too fast. If the level is low (logic level "0"), the comparison signal 811 indicates to control block 812 that the divided output frequency (f_{OUT}/N) ~~216~~ 218 is too slow. To synchronize the frequency comparison determination, the divide-by-N (÷N) counter 214 may be reset with respect to the timing signal ($R \bullet T_{REF}$) 814 so that the divided output frequency (f_{OUT}/N) 218 starts at the

initiation of the timing signal ($R \bullet T_{REF}$) 814. This reset synchronization is indicated in the cycles described in TABLE 2. It is noted that a "too fast" or "too slow" determination may also be made by directly comparing the reference frequency (f_{REF}) to the output frequency (f_{OUT}), if so desired.

On Pages 32-33, in the paragraph beginning at the bottom of Page 32:

As a general rule, the procedure in TABLE 2 operates by starting with a large capacitance value and in each cycle either dropping capacitance values, if the divided output frequency (f_{OUT}/N) ~~216~~ 218 is too slow, or keeping capacitance values, if the divided output frequency (f_{OUT}/N) ~~216~~ 218 is too high. In this manner, each successive cycle keeps or drops various capacitance values until the end of the procedure is reached. As depicted in Cycle 13 of TABLE 2, more capacitance than just the largest capacitance value (C[10]) may be initially included, if desired, to slow down the initial output frequency when the actual frequency is generally most uncertain.

On Pages 35-36, in the paragraph beginning at the bottom of Page 35:

FIG. 9C also depicts an embodiment for avoiding the problem with possible forward biasing of the diode (D_i) 906 when the NMOS transistor (S_i) 908 is in its "off" state. The PMOS transistor 916, which has its drain and source terminals connected between signal line 414 and node 917, avoids this "off" state diode problem by keeping the voltage at node 917 from floating when transistor 908 is in its "off" state. This PMOS transistor 916 is controlled by a signal ~~(B_i_hat) 916~~ (B_i_hat) 918 that is identical to the control signal (B_i) 910, except that the "_hat" designation represents that the signal ~~(B_i_hat) 916~~ (B_i_hat) 918 has a regulated voltage when high. In other words, signal ~~(B_i_hat) 916~~ (B_i_hat) 918 may only rise to a predetermined voltage level. Thus, when the bit (B_i) 910 goes to a high logic level, the signal ~~(B_i_hat) 916~~ (B_i_hat) 918 will only go to the regulated high voltage level. The addition of PMOS transistor 916 connects what would otherwise be an uncontrolled and potentially noisy floating node to a well-determined and quiet signal line 414. In this way, PMOS transistor 916 tends to eliminate the potential problem of the diode (D_i) 906 being forward biased due to a floating voltage at node 917.

On Page 39, in the first full paragraph:

For an RF1 output frequency with a maximum center frequency of about 2.0 GHz, the external inductor (L_{EXT}) may be about 2.0 nH. The two fixed capacitances (C_{FP}, C_{FN}) 410P and 410 N may each be about 2.0 pF. The summation of the eleven capacitance values within the positive side discretely variable capacitance (C_{DP}) 402P and the eleven capacitance values within the negative ~~positive~~ side discretely variable capacitance (C_{DN}) 402N may each be about 7.5 pF. Each of these eleven capacitance values are weighted as indicated in TABLE 1 with the unit weight (C_0) being equal to the total capacitance of 7.5 pF divided by the total of the weightings, which as set forth in TABLE 1 is 677. The summation of the widths for each eleven groupings of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 may be 1280 μm, 1280 μm, and 3840 μm, respectively. Each of the eleven transistor width values are weighted according to the weights given their respective capacitors (C_{DPi}, C_{DNi}) 902P and 902N in TABLE 1 with the unit transistor width being equal to the total width of 1280 μm or 3840 μm divided by the total of the weightings of 677. (It is noted that the technique depicted in FIG. 9C is utilized for any of the smallest transistor widths that fall below the minimum width allowed by the semiconductor manufacturing process utilized.) The transistor lengths are not varied and are all 0.35 μm. The total impedance for all of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 is about 0.56 Ω for worst case conditions.

On Pages 39-40, in the paragraph beginning at the bottom of Page 39:

For an RF2 output frequency with a maximum center frequency of about 1.3 GHz, the external inductor (L_{EXT}) may be about 3.1 nH. The two fixed capacitances (C_{FP}, C_{FN}) 410P and 410 N may each be about 3.6 pF. The summation of the eleven capacitance values within the positive side discretely variable capacitance (C_{DP}) 402P and the eleven capacitance values within the negative ~~positive~~ side discretely variable capacitance (C_{DN}) 402N may each be about 11.1 pF. Each of these eleven capacitance values are weighted as indicated in TABLE 1 with the unit weight (C_0) being equal to the total capacitance of 11.1 pF divided by the total of the weightings, which as set forth in TABLE 1 is 677. The summation of the widths for each eleven groupings of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 may be 1568 μm,

1568 μm, and 4704 μm, respectively. Each of the eleven transistor width values are weighted according to the weights given their respective capacitors (C_{DPi}, C_{DNi}) 902P and 902N in TABLE 1 with the unit transistor width being equal to the total width of 1568 μm or 4704 μm divided by the total of the weightings of 677. (It is noted that the technique depicted in FIG. 9C is utilized for any of the smallest transistor widths that fall below the minimum width allowed by the semiconductor manufacturing process utilized.) The transistor lengths are not varied and are all 0.35 μm. The total impedance for all of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 is about 0.46 Ω for worst case conditions.

On Pages 40-41, in the paragraph beginning at the bottom of Page 40:

For an IF output frequency with a maximum center frequency of about 600 MHz, the external inductor (L_{EXT}) may be about 6.7 nH. The two fixed capacitances (C_{FP}, C_{FN}) 410P and 410 N may each be about 8.0 pF. The summation of the eleven capacitance values within the positive side discretely variable capacitance (C_{DP}) 402P and the eleven capacitance values within the negative ~~positive~~ side discretely variable capacitance (C_{DN}) 402N may each be about 23.8 pF. Each of these eleven capacitance values are weighted as indicated in TABLE 1 with the unit weight (C_0) being equal to the total capacitance of 23.8 pF divided by the total of the weightings, which as set forth in TABLE 1 is 677. The summation of the widths for each eleven groupings of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 may be 3200 μm, 3200 μm, and 9600 μm, respectively. Each of the eleven transistor width values are weighted according to the weights given their respective capacitors (C_{DPi}, C_{DNi}) 902P and 902N in TABLE 1 with the unit transistor width being equal to the total width of 3200 μm or 9600 μm divided by the total of the weightings of 677. (It is noted that the technique depicted in FIG. 9C is utilized for any of the smallest transistor widths that fall below the minimum width allowed by the semiconductor manufacturing process utilized.) The transistor lengths are not varied and are all 0.35 μm. The total impedance for all of the transistor switches (S_{Pi}, S_{Ni}, S_{PNi}) 908P, 908N and 1210 is about 0.22 Ω for worst case conditions.

On Pages 41-42, in the paragraph beginning at the bottom of Page 41:

FIG. 16 illustrates the PLL 1500 of FIG. 15 during the fine tuning mode of operation (i.e. after coarse tuning is completed). In FIG. 16, only the analog control portions of the PLL

are shown. As shown in FIG. 16, a VCO 400 (such as, for example, VCO 400 of FIG. 4) provides an output frequency (f_{out}) 102. As shown in FIG. 16, the VCO input control signals 408 of FIG. 4 have been replaced by a M+1 voltage control inputs 1514. The output 102 is provided through control line 1508 to the divide-by-N circuit 214. An output 1510 of the divide-by-N circuit 214 is provided to a shift register 1504. The shift register 1504 is clocked by the output 1570 of the divide-by-Q block 1550 as shown. Parallel outputs 1520[0, 1, 2, ... M-1, M] of the shift register 1504 are provided to the phase detector / sample hold circuit 1502. The output 1530 of the divide-by-R circuit 204 is also provided to the phase detector. As will be described in more detail below, each of the outputs 1520 of the shift register 1504 has the same frequency (f_{OUT}/N), i.e. the update rate of the PLL, but is incrementally shifted in phase from each other. The phase detector / sample hold circuit 1502 detects the phase differences between the output 1530 of the divide-by-R circuit 204 and each of the outputs 1520[0, 1, 2, ... M] of the shift register 1504. Outputs 1512[0, 1, 2, ... M] of the phase detector / sample hold circuit 1502 provide control voltages indicative of the detected phase differences. These control voltages are in turn coupled to the inputs 1514[0, 1, 2, ... M-1, M] of the VCO 400 through which fine tuning control of the VCO may be achieved (as described below). Thus, rather than the VCO 400 being provided a single analog control voltage, a plurality of control voltages may be provided. As discussed below, in one embodiment twenty outputs may be provided from the shift register to generate twenty outputs of the phase detector / sample hold circuit 1502 and twenty inputs to the VCO. Because the shift register 1504 produces a series of outputs, each shifted in phase, the control voltages provided to the VCO will be a series of voltages offset from each other.

On Pages 44-45, in the paragraph beginning at the bottom of Page 44:

As noted above with reference to FIG. 17C, a plurality of the capacitance circuits (C_{A0}, C_{A1}, ... C_{AM}) may be utilized and the continuously variable capacitance C_A 406 is a result of the summation of the individual capacitance circuits. The overall conductance ($G_{equivalent}$ for C_A) of all of the capacitance circuits operating together, however, does not increase beyond the $G_{equivalent}$. FIG. 18 demonstrates this concept. FIG. 18 demonstrates ~~$G_{equivalent}$~~ $\omega C_{equivalent}$ vs. $G_{equivalent}$ over for the continuously variable capacitance C_A 406. As shown in FIG. 18 for illustrative purposes, the additive effect of incrementally fully turning on each transistor T_0, T_1, ... T_M is displayed. As can be seen, the total capacitance range for C_A (ΔC_A) (the sum of the ranges of the individual capacitance circuits) may be relatively large,

without a corresponding large change in conductance. This characteristic of the circuit of FIG. 17C helps minimize phase noise since the phase noise for the circuit is proportional to $G_{equivalent}$. Thus, a wide capacitance range for the continuously variable capacitance C_A 406 is provided without causing excessive phase noise. It may also be noted that as the control voltage on each control line 1514[0, 1, ... or M] changes from rail to rail, only a fraction of the total capacitance range is changed (i.e. where M+1=20 only $1/20^{th}$ of the total capacitance range). Thus, noise on any one particular control line will only have a minimal impact on the total capacitance C_A.

On Page 49, in the second full paragraph:

As mentioned above with reference to FIG. 22, only one transistor 2320 is turned on at any given time. Multiple transistors 2320 are provided so that a selectable resistance between the V_{PHASE} line 2200 and ground may be provided. In this manner the rate of decay of V_{PHASE}. The rate of decay will impact the number of individual capacitance circuits C_{A0}, C_{A1} ... C_{AM} which are operating in their active range at any given time. The desired gain is controlled by selectively providing a high signal on one of the SEL1, SEL2, SEL3, or SEL4. In this manner, only one of the AND gates 2306, 2308, 2310, ~~2312 and 2314~~ and 2312 will provide a high output, and thus, only one of the transistors 2320 will turn on and off in response to the rising and falling edges of the signals on lines 1530 and 1520[0].

On Page 50, in the second full paragraph:

FIG. 24C illustrates a timing diagram for the phase detector / sample hold circuit 1502. In FIG. 24C the operation of the charge switch 2302, V_{NOM} switch ~~2356~~ 2350 and sample / hold switch 2304 are shown in relation to the f_{REF}/R output 1530 and the shift register outputs 1520[0, 1, ... M]. As shown in FIG. 24C, the falling edges of the M+1 outputs of the shift register are each incrementally out of phase of the adjacent output. All of the signals in FIG.24C except the shift register outputs are clocked by the reference clock 106 (f_{REF}). The period of the reference clock is shown in the figure as T_{REF}.

On Pages 50-51, in the paragraph beginning at the bottom of Page 50:

As discussed above, FIG. 22 shows a portion of the phase detector / sample hold circuit 1502 for performing the phase detection for one of the outputs of the phase detector / sample hold circuit 1502. To perform the multi-line phase detection of FIG. 16, a plurality of the circuits 1502[0] of FIG. 22 may be used as shown in FIG. 25. In the circuit of FIG. 25, the resistors R1, R2, R3, ~~R4, and R5~~ and R4, transistors 2320, and gates 2306, 2308, 2310, ~~2312, and 2314~~ and 2312 shown in FIG. 22 have been combined in control blocks 2502 for ease of illustration. In operation, each of the charge switches 2302 operates in unison and each of the sample / hold switches 2304 operates in unison. Likewise all the SEL signals are applied together. Thus, during one phase detection cycle, the phase difference between the divide-by-R output signal 1530 and each of the falling edges of the M+1shift register outputs 1520 is detected and applied to the phase detector / sample hold outputs 1512. Because falling edges of each of the shift register output 1520[0, 1, ... M] are incrementally out of phase with the adjacent output, each of the phase detector / sample hold outputs 1512[0, 1, ... M] will be at different voltage level.